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ABSTRACT OF THE DISCLOSURE

An apparatus for indicating clock skew within integrated circuits (ICs) of a system. There are first and second IC chips operating on respective clocks in the system. According to the invention, the first IC chip operating on a first clock is configured to provide the first clock as output. The second IC chip operating on a second clock has a detection circuit to receive as input the first and the second clocks and to generate a compare signal as output, where the width of the compare signal is proportional to the amount of skew between the input clocks. The second IC chip also includes a sampling circuit coupled to receive the compare signal. With the sampling circuit, an output signal indicative of skew existing between the first and the second clocks can be asserted according to the compare signal.